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1. A bandwidth divider for allocating bandwidth between a plurality of packet processors, comprising:
 - (a) plurality of counters for measuring the bandwidth of data packets transferred from the bandwidth divider to a respective packet processor; and
 - (b) a controller for analyzing the plurality of counters and; transferring a data packet to a selected packet processor based on the contents of the plurality of counters.
 2. The bandwidth divider of claim 1, wherein the bandwidth divider includes a plurality of interfaces, each coupled to an input and output stream.
 3. The bandwidth divider of claim 2, wherein the plurality of counters includes a counter for each input stream/packet processor combination.
 4. The bandwidth divider of claim 2, further comprising a plurality of queues, one for each input stream/packet processor combination, each queue operable to receive packets and forward packets stored therein in accordance with the selection of the controller.
 5. The bandwidth divider of claim 4, wherein the input stream/packet processor combinations are organized as linked lists in a common memory pool.
 6. The bandwidth divider of claim 1, wherein the packet processor is a packet forwarding engine.
 7. The bandwidth divider of claim 1, wherein a counter indicates the level of bandwidth consumption of a packet processor.
 8. The bandwidth divider of claim 7, further comprising a decrement engine operable to decrement the indication of the level of bandwidth consumption of the packet processor is decremented over time.

9 The bandwidth divider of claim 8, wherein the decrementation is performed in accordance with a half-life decay function.

5 10. The bandwidth divider of claim 7, further comprising a normalizing engine operable to normalize the indication of the level of bandwidth consumption of the packet processor after each packet is processed.

10 11. The bandwidth divider of claim 10, wherein the indication of the level of bandwidth consumption of the packet processor is normalized such that the lowest indication for all counters is 0.

12. The bandwidth divider of claim 7, wherein the controller transfers a data packet to the packet processor with the lowest bandwidth consumption.

15 13. The bandwidth divider of claim 7, further comprising a random selector, wherein if the controller determines that a plurality of packet processors have an identical, lowest bandwidth consumption, the controller transfers the data packet to one of the plurality packet processors having the lowest bandwidth consumption randomly selected by the random selector.

20 14. The bandwidth divider of Claim 13, wherein the random selector includes a Linear Feedback Shift Register function and the controller is operable to transfer the data packet in accordance with the Linear Feedback Shift Register function.

25 15. A router comprising:

- 30 (a) a plurality of bandwidth dividers for receiving a first set of input streams and providing a first set of output streams;
- (b) a plurality of packet processors for receiving the first set of output streams from the bandwidth dividers and providing a second set of input streams;
- (c) a plurality of counters for monitoring the flow of data from the bandwidth dividers to the packet processors;

- (d) a controller for monitoring the counters and allocating the streams of data between the packet processors; and
- (e) a plurality of cross-bars for receiving the second set of input streams from the packet processors, multiplexing the second set of input streams, and providing a second set of output streams.

16. A method of directing data packets to a plurality of packet processors, comprising the steps of:

- monitoring the bandwidth consumed by the packet processors;
- determining, based on the bandwidth consumed by the packet processors, which packet processor has consumed the least amount of bandwidth;
- allocating a next data packet to the packet processor which has consumed the least amount of bandwidth.

17. The method of claim 16, further including incrementing counters to track the bandwidth consumed by the packet processors.

18. The method of claim 16, further including incrementing one counter for each input and output pair to track the bandwidth consumed by the packet processors.

19. The method of claim 17, wherein the determining step includes comparing the counters to ascertain the counter with the lowest value.

20. The method of claim 19, wherein:

- the determining step further includes determining if two or more counters have the identical, lowest value; and
- the allocating step further includes, if two or more counters have the identical, lowest value, allocating the data packet randomly as between the packets with the identical, lowest value.

21. The method of claim 17, including decrementing the counters over time.

22. The method of claim 17, including decrementing the counters over time using a half-life decay function.

5 23. The method of claim 17, including normalizing the counters.

24. The method of claim 17, including normalizing the counters by subtracting the value of the lowest counter from all counter values.

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